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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SNYDER, STEVEN G	

ART UNIT	PAPER NUMBER
2184	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,117	VAN GASSEL ET AL.	
	Examiner	Art Unit	
	STEVEN G. SNYDER	2184	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,9-14 and 20* is/are rejected.

7)☒ Claim(s) *4-8 and 15-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is in response to communication filed on April 30, 2009.

Status of Claims

Claims 1 – 20 are pending, of which claims 1, 9, and 13 are in independent form.

Response to Arguments

1. Applicant's arguments, see page 9 line 3 – page 10 line 31, filed April 30, 2009, with respect to the rejection of claims 1 – 3, 9 – 14, and 20 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of Houston, U.S. Patent 5,615,162.

Claim Objections

2. Claim 2 is objected to because of the following informalities: Claim 2 states "switching on memory banks and/or memory ICs of said buffer memory" in lines 2 – 3 of the claim. The first instance of the term "ICs" should be stated as "Integrated Circuits (ICs)." Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 3, 9 – 14, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Houston, U.S. Patent 5,615,162 (hereinafter referred to as Houston) in view of Olsen et al., U.S. Patent Application 2005/0071561 (hereinafter referred to as Olsen), further in view of Gibbs et al., U.S. Patent Application 2002/0045961 (hereinafter referred to as Gibbs).

Referring to claim 1, Houston discloses "A method for adaptively minimizing the total power consumption of an apparatus comprising a subsystem comprising a mass storage device and a buffer memory" (Fig. 9, computer system 200 containing a hard disk device as well as cache memory 204 and off-chip memory 206. Also, column 5 line 65 – column 6 line 30, power savings is realized by selectively activating or inactivating memory blocks), "said method comprising the steps of: determining an optimum buffer size" (column 5 line 65 – column 6 line 30, if "by some method of computation" it is determined that only a subset of memory blocks is needed, the remaining blocks of memory would be disconnected from the power supply. Houston states "therefore, the amount of memory currently in active status may vary according to usage and may be dynamically changed or anticipated."); and "adjusting the buffer size of said buffer memory to said optimum buffer size", such that the power consumption is minimal (column 5 line 65 – column 6 line 30, power savings is realized by selectively activating or inactivating memory blocks).

Houston does not appear to explicitly disclose determining an optimum buffer size "for which the power consumption of said subsystem is a minimum."

Houston discloses minimizing buffer memory power usage only.

However, Olsen discloses that "it is known that accessing a main storage device such as an HDD 106 consumes more energy than accessing information stored in random-access media such as the main memory 104" ([0025]). Thus, it can be seen that minimizing a buffer memory's size can have the effect of increasing the power utilized by a subsystem, since the main storage device, which requires more power than the buffer memory, would be accessed more frequently.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to find an optimal buffer size based on power consumption of a subsystem made up of a hard disk drive and a buffer memory.

Houston and Olsen are analogous art because they are from the same field of endeavor, which is power saving in a storage system.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Houston and Olsen before him or her, to modify the teachings of Houston to include the teachings of Olsen so that a hard disk drive's power consumption would also be taken into account when determining which memory blocks are activated or inactivated.

The motivation for doing so would have been to save as much power as possible, while ensuring that one component's power saving method does not cause the entire system to increase power usage.

Neither Houston nor Olsen appears to explicitly disclose minimizing power consumption "for a given streaming bit-rate to/from said buffer memory."

However, as stated above, Houston does disclose "by some method of computation" it is determined that only a subset of memory blocks is needed and Houston discloses the amount of memory currently in active status may vary "according to usage" (column 5 line 65 – column 6 line 30).

While neither Houston nor Olsen appears to explicitly disclose utilizing a given streaming bit-rate to/from a buffer memory for determining an optimum buffer size for minimizing power consumption, Gibbs discloses deciding to activate a storage device depending on factors such as the data transfer rate of the storage device and a data sample rate ([0034]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include the data transfer rate as a factor in the method of computation described by Houston, since a method for determining a transfer rate of a storage device is a known.

Houston, Olsen, and Gibbs are analogous art because they are from the same field of endeavor, which is power saving in a storage system.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Houston, Olsen, and Gibbs before him or her, to modify the teachings of Houston and Olsen to include the teachings of Gibbs so that data transfer rates would be included in the computation of memory blocks needed to be powered.

The motivation for doing so would have been to save power in a system including memory (as taught by both Houston and Gibbs) by using a known method of determining transfer rate as the "method of computation" described by Houston.

Therefore, it would have been obvious to combine Gibbs with Houston and Olsen to obtain the invention as specified in the instant claim.

As per claim 2, Houston discloses "said step of adjusting the buffer size comprises switching on memory banks and/or memory ICs of said buffer memory for increasing the size of said buffer memory, and switching off memory banks and/or memory ICs for decreasing said buffer memory" (column 5 line 65 – column 6 line 30, power savings is realized by selectively activating or inactivating memory blocks).

As per claim 3, Houston discloses "the storage device is a hard disk drive" (Fig. 9).

Houston also discloses how, if "by some method of computation," it is determined that only a subset of memory blocks is needed, the remaining blocks of memory would be disconnected from the power supply. Houston further states "therefore, the amount of memory currently in active status may vary according to usage and may be dynamically changed or anticipated" (column 5 line 65 – column 6 line 30).

Neither Houston nor Olsen appears to explicitly disclose "the step of determining an optimum buffer size comprises: determining a hard disk drive data rate of the hard disk drive; determining the stream bit-rate to/from the buffer memory; and determining

the optimum buffer size having the lowest power consumption at the determined stream bit-rate."

However, Gibbs discloses deciding to activate a storage device depending on factors such as the data transfer rate of the storage device and a data sample rate ([0034]).

Houston, Olsen, and Gibbs are analogous art because they are from the same field of endeavor, which is power saving in a storage system.

At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Houston, Olsen, and Gibbs before him or her, to modify the teachings of Houston and Olsen to include the teachings of Gibbs so that a hard disk data rate and a streaming bit-rate would be included in the computation of memory blocks needed to be powered.

The motivation for doing so would have been to save power in a system including memory (as taught by both Houston and Gibbs) by using a known method of determining a hard disk data rate and a streaming bit-rate in Houston's "method of computation" for determining the amount of needed memory blocks, which varies "according to usage."

Therefore, it would have been obvious to combine Gibbs with Houston and Olsen to obtain the invention as specified in the instant claim.

Referring to claim 9, claim 1 recites corresponding limitations as that of claim 9. Therefore, the rejection of claim 1 applies to claim 9. Further limitations of claim 9 are discussed below.

Olsen discloses the circuit comprising "a processing unit" (Fig. 1, processor 102) and "retrieve the data from the mass storage device" ([0006], HDD and using DRAM as a read cache).

As per claim 10, Olsen discloses "An apparatus comprising a subsystem comprising mass storage device, a buffer memory" (Fig. 1, main storage device 106, main memory 104) "and the circuit according to claim 9 (see rejection to claim 9 and claim 1 above).

As per claim 11, Houston discloses "said buffer memory comprises SDRAM circuits having banks of memory adapted to be independently switched on/off" (column 1 lines 20 – 22 and column 5 line 65 – column 6 line 30, power savings is realized by selectively activating or inactivating memory blocks).

As per claim 12, Olsen discloses "a scheduler function executable by the processing unit controls accessing the storage device and the buffer memory" ([0024] and Fig. 1, arbiter or storage controller 116).

Referring to claim 13, claim 1 recites corresponding limitations as that of claim 9. Therefore, the rejection of claim 1 applies to claim 9. Further limitations of claim 9 are discussed below.

Also, Olsen discloses "A computer-readable medium having embodied thereon a computer program for processing by a computer, the computer program comprising code segments" (claim 18).

Note, claim 14 recites the corresponding limitations of claim 3. Therefore, the rejection of claim 3 applies to claim 14.

Note, claim 20 recites the corresponding limitations of claim 12. Therefore, the rejection of claim 12 applies to claim 20.

Allowable Subject Matter

5. **Claims 4 – 8 and 15 – 19** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent **5,719,800** discloses monitoring a duty cycle of a cache and throttling when necessary.

U.S. Patent **7,127,560** discloses dynamically controlling cache size.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN G. SNYDER whose telephone number is (571)270-1971. The examiner can normally be reached on Mon. - Thurs. 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dr. Henry Tsai can be reached on (571) 272-4176. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven G Snyder/
Examiner, Art Unit 2184

/Henry W.H. Tsai/
Supervisory Patent Examiner, Art Unit 2184